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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,655	05/10/2005	Christian Reichinger	DE02 0249 US	6552

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EXAMINER	
ALMO, KHAREEM E	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/534,655	REICHINGER, CHRISTIAN	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 9/27/2006 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (US 4291274).

With respect to claim 1, Figure 2 of Suzuki et al. discloses a phase comparator, providing regulating signals for a PLL module, and that compares a phase angle of a first input signal (SIG) with a second input signal (REF) by evaluating the edges of the first and the second input signals and generates reset signals (R) therefrom using a circuit, characterized in that at least one additional circuit (10 or 11) is provided that further evaluates, different edges of the first or the second input signals and generates therefrom additional reset signals (R), wherein each of the reset signals and each of the additional reset signals reset the regulating signals.

With respect to claim 2, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from rising and decaying edges of the first and the second input signals and in

that the additional circuit derives the additional reset signals from the rising and decaying edges of the first and the second input signals.

With respect to claim 3, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that a dedicated additional circuit is provided for each of the first and the second input signals (REF and SIG), with one of the dedicated additional circuit (10) evaluating the edges of the first input signal (REF) and the second additional circuit (11) evaluating the edges of the second input signal (SIG).

With respect to claim 4, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that another additional circuit (10 or 11) evaluates rising and decaying edges of one of the first and second input signal (REF) and the at least one additional circuit evaluates the rising and decaying edges of the other input signal (SIG).

With respect to claim 5, Figure 2 of Suzuki et al. discloses a phase comparator as claimed in claim 1, characterized in that output signals from the at least one additional circuits (10, 11 or 12) are applied to reset inputs of flip-flops (8 or 9) belonging to the phase comparator via a gate (12), there also being connected to the gate a gate (and gates to 8 and 9) to which the regulating signals are applied.

With respect to claim 6, Figure 2 of discloses a phase comparator as claimed in claim 1, characterized in that the at least one additional circuits each has two RS flip-flops and gates (10 and 11), which are integrated into the PLL module.

With respect to claim 7, Figure 16 of Suzuki et al. discloses a phase comparator that compares the phase angle of a first input signal (SIG) with a second input signal

(REF) by evaluating the edges of the input signals and generates reset signals therefrom, characterized in that at least one additional circuit (27 and 29) is provided that evaluates further, different edges of the input signal or signals and generates therefrom additional reset signals for the regulating signal or signals characterized in that the first and the second input signals (SIG and REF) are applied to the at least one additional circuit via an OR gate (from 28 and 30).

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsinker (US 6323692).

With respect to claim 1, Figure 10 of Tsinker discloses a phase comparator, providing regulating signals for a PLL module, and that compares a phase angle of a first input signal (FILTER CLOCK) with a second input signal (REF. CLOCK) by evaluating edges of the first and the second input signals and generates reset signals (RESET_DN and RESET_UP) therefrom using a circuit, characterized in that at least one additional circuit (202) is provided that further evaluates, different edges of the first or the second input signals and generates therefrom additional reset sigals (UPDN_RST), wherein each of the reset signals and each of the additional reset signals reset the regulating signals.

With respect to claim 2, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that the phase comparator obtains the regulating signals from rising and decaying edges of the first and the second input signals and in

that the at least one additional circuit derives the additional reset signals (UPDN_RST) from the rising and decaying edges of the first and the second input signals.

With respect to claim 3, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that a dedicated additional circuit (202 and 204) is provided for each of the first and second input signals (REF CLOCK and FILTER CLOCK), with one of the dedicated additional circuits (204) evaluating the edges of the first input signal (REF CLOCK) and the other dedicated additional circuit (202) evaluating the edges of the second input signal (FILTER CLOCK).

With respect to claim 4, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that another additional circuit (202) evaluates rising and decaying edges of one of the first and the second input signals (FILTER CLOCK) and the at least one additional circuit (204) evaluates rising and decaying edges of the other input signal (REF CLOCK).

With respect to claim 5, Figure 10 of Tsinker discloses a phase comparator as claimed in claim 1, characterized in that output signals (DN and UP) from the at least one additional circuits (204 and 202) are applied to reset inputs(RN) of flip-flops belonging to the phase comparator via a gate (216 and 218), there also being connected to the gate a gate (212 and 214) to which the regulating signals are applied.

Response to Arguments

5. Applicant's arguments filed 9/27/2006 have been fully considered but they are not persuasive.

With respect to applicants arguments that the Suzuki reference fails to cite any portion that corresponds to the claimed limitations directed to that each of the reset signals and each of the additional reset signals reset the regulating signals the Examiner disagrees. Since the next state Q controls the operation of the flip-flops and the operation of the additional circuit at R both reset the regulating signals.

With respect to applicants argument that Suzuki fails to teach or suggest limitations directed to the additional circuit to evaluate different edges of the first or second input signals and generate additional reset signals there from, the Examiner disagrees. The additional circuits as disclosed above evaluate the first and second input signals because they depend directly on the first and second input signals and also generate their reset signals from the first and second input signals.

With respect to applicants argument the Suzuki reference fails to teach that at least one additional circuit evaluates different edges of the first or second input signals as in the claimed invention the Examiner disagrees. Since a signal consists of several edges different edges can be interpreted as a different pulse of the same signal. This claim therefore can clearly correspond to the cited reference. The "R" of Figure 2 of the Suzuki reference is the R of different circuits. (i.e. the R of the first flip flop 9 is a different R from another flip-flip of 11 but both function with reset capabilities.) Furthermore since two different signals are evaluated in the feedback loop the additional circuits evaluate two different signals, which correspond to different edges (i.e. the edge of the first signal and the edge of the second signal.)

With respect to applicants argument the Suzuki reference fails to correspond to claimed limitations directed to that the first and second input signals are applied to the additional circuit via an OR gate the Examiner disagrees. The "OR" gate can be any one of the "OR" gates in flip flop 30 (which receive the Sig signal, outputs a signal into 51, then to 52 and then into 29), as well as in flip flop 28 (which receive the REF signal, outputs a signal into 51, then to 52 and then into 27), or the or gates inside of 27 and 29 themselves (using the broadest reasonable interpretation of via an OR gate).

With respect to applicants arguments the Tsinker reference fails to correspond to limitations directed to that each of the reset signals and each of the additional reset signals reset the regulating signals the Examiner disagrees. Because the RESET_UP signal and the RESET_DN signal depend on the input of the CLOCK and the FILTER CLOCK they can be understood to be resetting the regulating signals.

With respect to applicants arguments the Tsinker reference fails to teach limitations directed to the additional circuit to evaluate different edges of the first or the second input signals and generate additional reset signals there from the Examiner disagrees. Because they evaluate edges from different signals these edges can be considered to be different edges. Furthermore the UPDN_RST is generated by flip-flop 202 because the signal from 202 generates the signal coming from 210. Also each component can be considered as a circuit. Each component that adds a part of the signal can be said to generate the signal.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
12/10/06

Quan Tra
Primary Examiner